REMARKS

The Examiner rejected claims 25-42 under 35 U.S.C. §102(e) as being unpatentable over Bedmar et al. (U.S. Patent Publication 2004/0060023). Applicants respectfully point out that the first named inventor of (U.S. Patent Publication 2004/0060023) is Bednar not Bedmar and have, for clarity, corrected all subsequent references in this document including those of the Examiner. Applicants believe the Examiner intended to reject claims 21-42.

Applicant's amendment of claim 42 is not made in response to the Examiners rejection of claim 42, but rather to correct a typographical error.

Applicants respectfully traverse the §102(c) rejections with the following arguments.

35 USC § 102

Applicants point out the five inventers of United States Patent Publication 2004/0060023, namely, Thomas R. Bednar, Scott W. Gould, David E. Lackey Douglas W. Stout and Paul S. Zuchowski are the same five inventors as Patent Application S/N 10/604,277. Thus the rejections of claims 21-42 under 35 U.S.C. 102(e), to wit "(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent ..." is improper and must be withdrawn because the cited art (United States Patent Publication 2004/0060023) is not by another as 35 U.S.C. 102(e) requires. Further, MPEP 706.02(a) states "In order to apply a reference under 35 U.S.C. 102(e), the inventive entity of the application must be different than that of the reference."

As to claims 21 and 31, the Examiner states that "Bednar et al. disclose an electrical structure comprising: a parent terrain denoted as VO (see fig 1, fig 3 and fig 5 element 111 paragraph 0029); and N voltage islands denoted as V1 and V2 said voltage island V1 nested within said parent terrain VO and said voltage island V2 nested within said voltage island V1 (see fig 1, fig 3, and fig 5 paragraph 0034, and paragraph 0042 to 0050)."

Applicants contend that claim 21 is not anticipated by Bednar et al. because Bednar et al. does not teach each and every feature of claim 21. For example, Bednar et al. does not teach "said voltage island V_1 nested within said parent terrain V_0 and said voltage island V_2 nested within said voltage island V_1"

First, Applicants respectfully point out that there is no voltage island V2 in Bednar et al. In Bednar et al. FIG. 1, there is parent terrain 111 and a V1 voltage island 120 nested with the patent terrain, but there is no voltage island V2 nested with voltage island V1.

The term "voltage island" is described in Applicants paragraph [0023], to wit "The minimum hierarchal structure of every voltage island according to the present invention includes at least a VDDN power supply and voltage shifting means or fencing means or both voltage shifting means and fencing means. Additionally, every voltage island according to the present invention may further include state saving means, one or more switch elements, a VDDI power supply and associated power distribution network, a VDDSS power supply, and one or more voltage buffering circuits. If a voltage island serves as a parent terrain for another, nested voltage island, then VDDI of the parent voltage island will be the VDDO of the nested voltage island."

The power supplies "VDDN", "VDDI", "VDDO", "VDDSS" and the term "fencing" are defined in Applicants paragraph [0017], to wit "For the purposes of the present invention VDDN is defined as a general power supply provided to a voltage island, VDDI is defined as a power supply present within the voltage island and distributed through a network to devices within the voltage island, VDDO is defined as a power supply of the voltage islands parent terrain and VDDSS is defined as an optional power supply to support state-saving functions within the voltage island. ... Fencing is defined shifting the voltage level of specified circuits from VDDI to VDDO when a voltage island is powered down and from VDDO to VDDI when a voltage island is powered up." Applicants definitions of VDDO and VDDI are consistent with the definitions of VDDO and VDDI found in pasragraph [0027] of Bednar et al.

In FIG. 1 of Bednar et al., a parent terrain 111 supplies VDDN (VDDO in FIG. 1) and there is only one voltage island 120 connected to power supplies VDDO and having a distribution power network VDDI. There is a region 125 of state saving latches 125 (which are part of the fencing circuit taught by Bednar et al. and required by Applicants definition of a

voltage island) within voltage island 120, but region 125 is not another voltage island. Another voltage island nested within voltage island 120 would require a VDDN being either VDDO or VDDI and have an internal voltage distribution network VDDI different from the VDDO or VDDI of voltage island 120 and this does not exist in Bednar et al. FIG. 1. Note the dashed boundary around region 124 and also that Bednar et al. clearly teaches in paragraph [0027] "Item 124 illustrates a region of state-saving latches 125 used to store logic states during power-off periods." In fact, the latches 125 are the same latches as in Applicants claims 25 and 35, which the Examiner has cited as part of the fencing means.

Second, Applicants have examined Bednar et al. FIGs 3 and 5 and paragraphs [0029] and [0042] to [0050] and find no teaching of a voltage island nested within another voltage island as the Examiner has alleged. Bednar et al. at most teaches there can be multiple voltage islands, and all at the same hierarchal nesting level.

Based on the preceding arguments, Applicants respectfully maintain that claim 21 is not unpatentable over Bednar et al. and is in condition for allowance. Since claims 22-30 and 41 depend from claim 21, Applicants respectfully maintain that claims 22-30 and 41 are likewise in condition for allowance.

Applicants contend that the arguments present *supra* with respect to claim 21 are applicable to claim 31 and therefore maintain that claim 31 is not unpatentable over Bednar et al. and is in condition for allowance. Since claims 32-40 and 42 depend from claim 31, Applicants respectfully maintain that claims 32-40 and 42 are likewise in condition for allowance.

As to claims 41 and 42, the Examiner states that "Bednar et al. disclose further including: additional voltage islands denoted as V3, V4,....Vn, a voltage island Vz nested within a voltage

island Vz-1 for z = 3, 4,....N, wherein N is an integer of at least 3 (see fig 1, fig 3, and fig 5 paragraph 0034, and paragraph 0042 to 0050 and background)."

As stated *infra*, Applicants have not found a second voltage island nested with a first island, no less a third voltage island nested within the second voltage island. Applicants can not find such a teaching in Bednar et al. FIGs. 1, 3 or 5, or in paragraphs [0034] and [0042] to [0050] or in the background.

Applicants contend that the arguments present *supra* with respect to claim 41 are applicable to claim 42 and therefore maintain that claims 41 and 42 are not unpatentable over Bednar et al. and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Bednar et al.

Dated: 10/19/2005

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